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EXAMINER
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2675	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/522,428	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 152* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 152* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4, 7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 68, 75, and 83 are objected to because of the following informalities: Claims 68 and 75 are identical. Claim 83 is listed twice, once dependant on claim 2 and once on claim 4. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 – 152 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 3, 5, and 7 state that the voltage gray scale method and the time ratio gray scale method are conducted simultaneously. Claims 2, 4, 6, 8 state that the voltage gray scale method is conducted first and the time ratio gray scale method is conducted next. The phrases "conducted simultaneously" and "conducted next" are confusing and ambiguous. Whether using a time ratio gray scale method or a voltage gray scale method, the individual pulses have both a voltage dimension and a time dimension. Using the voltage scale method, each pulse has a time scale dimension, and when using a time ratio gray scale method, each pulse has a voltage. Therefore, it is misleading to state that both are either conducted simultaneously or conducted next without additional information.

Claims 9 – 152 are rejected as dependant on rejected claims 1 – 8.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada et al., USPN 5,673,061 [EP 0 655 726 A].

Claim 1

Claim 1 describes a display device.

Okada teaches a display device with an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix. Okada, col. 9, lines 34 – 35; col. 9, lines 57 – 58; and figure 1.

Okada teaches a source driver [data driver 102] and a gate driver [scanning driver 103] to drive the active matrix circuit. Okada, col. 9, lines 51 – 60; and figure 1.

Okada teaches that n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method, V_0, V_8, V_{16}, V_{24}, V_{32}, V_{40}, V_{48}, V_{56}, and V_{64}; (m-n) bit information is used for a time ratio gray scale method, $t_0 - t_7$. Okada, col. 11, lines 33 – 37; col. 12, lines 14 - 16; and figure 6. In the example given, m equals 12, n equals 8. Thus, both m and the n are integers equal to or larger than 2. It is inherent that m>n if (m-n) bit information is used for a time ratio gray scale method.

Okada teaches that the voltage gray scale method and the time ratio gray scale method are conducted simultaneously. Okada, col. 18, line 57 – col. 20, line 18, and figure 14.

Claim 11

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

6. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Okumura, USPN 5,363,118.

Claim 2

Claim 2 describes a display device.

Okumura teaches a display device comprising an active matrix circuit comprising a plurality of pixel TFTs disposed in matrix. Okumura, col. 1, lines 7 – 10, 31 – 39.

Okumura teaches a source driver 304 and a gate driver 302 which drive the active matrix circuit. Okumura, figure 1.

Okumura teaches n bit information, D1, D2, D3, out of m bit digital video data, D1 –D5, inputted from an external is used for a voltage gray scale method. Okumura, col. 5, lines 19 – 29 and figures 4 and 5. Okumura teaches (m-n) bit information, D4, D5, is used for a time ratio gray scale method. Okumura, col. 5, lines 30 – 48, and figures 4 and 5. In the example given, m is 5 and n is 3. Thus both m and n are integers equal to or larger than 2. It is inherent that m>n.

Claim 2 states that the voltage gray scale method is conducted first and the time ratio gray scale method is conducted next. Okumura teaches,

> The digital data D4 and D5 select any one of timing control signals A, B and C thereby the analog switch 106 is operated to turn OFF. The timing control of the off performance of the analog switch 106 determines any one of the voltage

> levels E5, E51, E52 and E53, followed by storing in the pixel capacitor 114. When the digital data D4 and D5 are "0" and "0" respectively, the voltage level E5 is selected. When the digital data D4 and D5 are "0" and "1" respectively, the voltage level E51 is selected. The pixel has a gray level corresponding to the selected voltage level. The novel multi-level driver operation of this embodiment permits the thirty two gray level display to be accomplished by the eight external power supplies 103.

Okumura, col. 6, lines 23 – 37; and figure 5.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 3, 7, 34, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. in view of Yasunishi, USPN 6,094,243.

Claim 3

Claim 3 describes a display device similar to claim 1 but adds that one frame image comprises 2^{m-n} subframes. Although Okada does not specifically state this formula, it uses the formula to determine the number of required gray-scale voltages. Okada, col. 2, lines 15 – 22.

Okada, however, does not specifically describe subframes.

Yasunishi teaches dividing a period T into k subframes with 2^k levels. Yasunishi, col 8, lines 44 – 67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine k subframes with 2^k levels with the display device of Okada to produce a display

device that has each frame image comprising 2^{m-n} subframes. Yasunishi invites such combination by teaching,

> There are provided subframes of a number greater than the bit length of data (i.e., the number of gray-scale bits) which represent the gray-scale levels of input image data. A period and a voltage value are set independently for each subframe, whereby a certain number of gray-scale levels can be effected with a lesser number of subframes as compared to the conventional frame modulation method. Moreover, by setting the period and the voltage value independently for each subframe, it is possible to avoid the reduction in the minimum pulse width which would occur in the conventional pulse width modulation method as the number of gray-scale levels increases. As a result, flickers in the displayed images and the display non-uniformity caused by the waveform distortion can be suppressed.
>
> Furthermore, image data for one frame is processed as binary display data which is set independently for each subframe. Therefore, it is possible to eliminate the complicated large-scale arithmetic circuit for performing square-sum calculation and square-root extraction, and a high-precision liquid crystal driver for outputting the analog voltage amplitude, which are required in the conventional amplitude modulation method.
>
> Furthermore, by setting a voltage amplitude independently for each subframe, it is possible to construct a display device most suitable for the response performance of the liquid crystal panel and the voltage endurance of the liquid crystal driver.
>
> Thus, the invention described herein makes possible the advantages of: (1) providing a liquid crystal display device capable of conducting a gray-scale display while suppressing flickers in the displayed images which would occur in the frame modulation method and suppressing the display non-uniformity which would occur in the pulse width modulation method, without increasing the circuit scale so significantly as in the amplitude modulation method; and (2) providing a method for driving such a liquid crystal display device.

Yasunishi, col. 6, line 52 – col. 7, line 21.

Claim 7

See discussions of claims 1 and 3 above and claim 5 below.

Claims 34 and 38

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Yasunishi.

Claim 4

Claim 4 describes a display device similar to claim 2 but adds that one frame image comprises 2^{m-n} subframes. Okumura teaches that one frame image comprises 2^{m-n} voltage levels. Okumura, col. 6, lines 38 – 56.

Okumura does not specifically describe these voltage levels as subframes.

For the reasons given in the discussion about claim 3 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine k subframes with 2^k levels with the display device of Okumura to produce a display device that has each frame image comprising 2^{m-n} subframes.

10. Claims 5, 10, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al.

Claim 5

Claim 5 describes a display device similar to claim 1 but adds that an image is displayed by an image gray scale of $(2^m-(2^{m-n}-1))$ patterns.

Okada does not specifically teach an image gray scale of $(2^m-(2^{m-n}-1))$ patterns.

Okada teaches that patterns that between the specified pair of gray-scale voltages, $(2^y -1)$ intermediate voltages can be obtained. Therefore, the number of obtainable intermediate voltage is $2^x (2^y - 1)$, where x plus y equals the number of bits, with x the number of upper bits and y the number of lower bits. Okada, col. 15, line 51 – col. 16, line 33; col. 24, line 50 – 65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the formula of Okada to obtain the same results as obtained by the formula $(2^m-(2^{m-n}-1))$. But definition, x equals m – n; y equals n. Thus, for m = 6 and n = 3, according to the claim 5 the image gray scale has 57 patterns. According to Okada, the number of intermediate voltages is 56. However, the Okada formula excludes the zero or black value of 000000. If the black value is added to Okada, the image gray scale has 56 plus 1 for 57 patterns. For m = 5 and n = 2, according to claim 5 the image gray scale has 25 patterns. According to Okada, the number of intermediate voltages is 24 plus the black value of 1 for 25 patterns.

The claim 5 formula can be derived from the Okada formula as follows.

According to Okada, the number of obtainable intermediate voltages is $2^x (2^y - 1)$.

Thus, the number of image gray scale patterns with the black value is $2^x (2^y - 1) + 1$.

Since x = m – n and y = n, then

$$2^x (2^y - 1) + 1 = 2^{m-n} (2^n - 1) + 1 = 2^{m-n+n} - 2^{m-n} + 1 = 2^m - 2^{m-n} + 1 = 2^m-(2^{m-n}-1)$$

Therefore, the claim 5 formula is identical to the Okada formula.

Claim 10

Claims 10, 27, 29, and 31 teach that m is 8 and the n is 2.

Okada does not specifically teach that m is 8 and n is 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to create the display device of Okada where m is 8 and n is 2. Okada invites such teaching,

> In the driving circuit in Example 1 described above, a pair of gray-scale voltages are specified from the plurality of gray-scale voltages, based on the upper three bits D_5, D_4, and D_3 of the 6-bit video data D_0, D_1, D_2, D_3, D_4, and D_5. A pair of analog switches corresponding to the specified pair of gray-scale voltages are driven at a duty ratio corresponding to the lower three bits D_2, D_1, and D_0. However, the invention is not limited to this manner.

Okada, col. 15, lines 43 – 50.

> In this example, the number of the oscillating signals t_0 - t_4 has been assumed to be equal to the number of lower bits (i.e., 5) used for specifying the oscillating signal T of the 8-bit video data. However, the invention is not limited to this specific case. For example, some of the oscillating signals t_0 - t_4 can be omitted, because the omitted oscillating signal(s) can be generated by repeatedly using the remaining oscillating signals. Also, the duty ratio of the oscillating signal is not limited to the above-described example.

Okada, col. 21, lines 33 – 41.

Claim 36

Okada teaches, in an example, that m is 12 and n is 4. Okada, col. 2, line 37 – col. 3, line 20; and figures 22 and 23.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Okada.

Claim 6

Claim 6 describes a display device similar to claim 2 but adds that an image is displayed by an image gray scale of $(2^{m}-(2^{m-n}-1))$ patterns.

Okumura does not specifically teach an image gray scale of $(2^{m}-(2^{m-n}-1))$ patterns.

As discussed in the response to claim 5 above, the Okada formula is the same as the $(2^m-(2^{m-n}-1))$ pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the Okada formula to determine the image gray scale of the display device of Okumura. Okada teaches,

> In general, the present invention can be applied to a driving circuit for driving a display apparatus in accordance with (x+y) bits. The display apparatus displays an image with $2^{(x+y)}$ gray scales. Herein, x and y are desired positive integers. In the driving circuit according to the invention, a pair of gray-scale voltages among a plurality of gray-scale voltages are specified, based on a value represented by the upper x bits. The required number of gray-scale voltages is $(2^x + 1)$, and a gray-scale voltage pair is specified from 2^x gray-scale voltage pairs. A pair of analog switches corresponding to the specified gray-scale voltages are driven at a duty ratio corresponding to a value represented by the lower y bits. As a result, between the specified pair of gray-scale voltages, $(2^y - 1)$ intermediate voltages can be obtained. Therefore, the number of obtainable intermediate voltage is $2^x (2^y - 1)$. The mean values of these intermediate voltages are different from each other.

Okada, col. 15, lines 51 – 67. Since the Okumura circuit is nearly identical to Okada, the Okada formula would also apply to Okumura for the same reasons.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Yasunishi and Okada.

Claim 8

See discussions of claim 2, 4, and 6 above.

13. Claims 12 – 17, 27, 29, 31, 41, 43, 45, 48, 50, 52, 55, 57, 59, 62, 64, 66, 69, 71, 73, 77, 79, 81, 89, 91, 93, 95, 97, 99, 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 121, 123, 125,

127, 129, 131, 133, 135, 137, 139, 141, 143, 145, 147, 149, and 151 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., 6,335,716 B1, or Holmes et al., USPN 3,792,919, or Kimura, USPN 5,610,741, or Munyan, USPN 5,761,485, or Stambolic et al., USPN 5,893,798, or Kleinschmidt et al., USPN 6,085,112, or Sato, USPN 6,167,208, or Yun et al., USPN 5,835,139, in view of Okada et al as applied to claim 1 or claim 5 above, or of Okada et al and Yasunishi as applied to claim 3 or claim 7 above.

First Set of Appliance Claims

As to claims 12, 41, 43, and 45, Yamazaki teaches a rear projector comprising three display devices Yamazaki, col. 16, lines 1 – 25; and figure 11. As to claims 13, 48, 50, and 52 Yamazaki teaches a front projector comprising three display devices. Yamazaki, col. 15, lines 32 – 56; and figure 10. As to claims 14, 55, 57, and 59, Holmes teaches a single plate type rear projector. Holmes, col. 8, lines 48 – 58. As to claims 15, 62, 64, and 66, Yamazaki teaches a goggle type display comprising two display devices. Yamazaki, col. 26, lines 38 – 40; and figure 22D. As to claims 16, 69, 71, and 73, Kimura teaches a display for portable information terminal. Kimura, col. 1, lines 11 – 16. As to claims 17, 77, 79, and 81, Yun et al., teaches a notebook type personal computer. Yun, col. 1, lines 49 – 52; and figure 9. As to claims 89, 91, 93, and 95, Yamazaki teaches a mobile telephone. Yamazaki, col. 26, lines 26 – 29. As to claims 97, 99, 101, and 103, Yamazaki teaches a video camera. Yamazaki, col. 26, lines 29 – 33; and figure 22B. As to claims 105, 107, 109, and 111, Yamazaki teaches a mobile computer. Yamazaki, col. 26, lines 34 – 37; and figure 22C. As to claims 113, 115, 117, and 119, Munyan teaches a portable electric book. Munyan, col. 1, lines 56 – 57. As to claims 121, 123, 125, and 127, Kimura teaches a personal computer. Kimura, col. 1, lines 11 – 16. As to claims 129, 131,

133, and 135, Stambolic et al. teaches a electronic game device. Stambolic, col. 1, lines 9 – 10. As to claims 137, 139, 141, and 143, Kleinschmidt teaches an image reproduction device. Kleinschmidt, col. 5, lines 58 – 61. As to claims 145, 147, 149, and 151, Sato teaches a digital camera. Sato, col. 1, lines 7 – 10.

None of these patents specifically teach the display device of Okada.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the display device of Okada for these generally small appliances. Okada teaches,

> Accordingly, it is unnecessary to provide an additional driving circuit depending on the cases where the driving circuit directly outputs one of the plurality of gray-scale voltages and where the driving circuit alternately outputs the specified pair of gray-scale voltages. As a result, it is possible to simplify the configuration of the driving circuit, and the size of the driving circuit can be minimized.
>
> Thus, the invention described herein makes possible the advantage of providing a driving circuit for a display apparatus, which has a simplified and small construction, and which can display an image with multiple gray scales in accordance with multi-bit video data.

Okada, col. 7, line 59 – col. 8, line 3.

14. Claim 26, 28, 30, 32, 33, 35, 37, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura as applied to claim 2 above, or Okumura in view of Yasunishi as applied to claim 4 above, or Okumura in view of Okada et al. as applied to 6 above, or of Okumura in view of Okada et al. and Yasunishi as applied to claim 8 above.

Claims 26, 26, 28, 30, 32, 33, 35, 37, and 39

Claims 26, 28, 30, and 32 add that m is 8 and n is 2. Claim 33, 35, 37, and 39 add that m is 12 and n is 4. Okumura gives an example where m is 5 and n is 3.

Okumura does not specifically teach that m is 8 or 12 or that n is 2 or 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to vary the m and the n in Okumura. Okumura invites such by teaching,

> While in the above embodiment the thirty two gray level display is accomplished, the number of the gray levels may readily be expanded by modifications of timing control signals and digital data to be allocated to the logic circuit. When digital signals of m-bits are allocated for each pixel, n-bit signals involved in the m-bit signals are allocated to the address recorder to select any one of 2^n power supplies. Remaining digital signals of (m-n) bits are allocated to the logic circuits to select any one of a plurality of timing control signals. The timing control of the off switching performance of the analog accomplished by the timing control signal determines any one of 2^{m-n} voltage levels, each of which is increased from the predetermined voltage supplied by the selected power supply. The number of gray levels is equivalent to 2^n of the external voltage supplies multiplied by 2^{m-n} of variable voltage levels controlled by the switching performance of the analog switch 106. Thus, the 2^m gray level display may be realized.

Okumura, col. 6, lines 38 – 56.

15. Claims 40, 42, 44, 46, 47, 49, 51, 53, 54, 56, 58, 60, 61, 63, 65, 67, 68, 70, 72, 74, 75, 76, 78, 80, 82, 90, 92, 96, 98, 100, 102, 104, 106, 108, 110, 112, 114, 116, 118, 120, 122, 124, 126, 128, 130, 132, 134, 136, 138, 140, 142, 144, 146, 148, 150, and 152 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. or Holmes et al. or Kimura or Munyan or Stambolic et al. or Kleinschmidt et al. or Sato or Yun et al. in view of Okumura as applied to claim 2 above, or Okumura in view of Yasunishi as applied to claim 4 above, or Okumura in view of Okada et al. as applied to 6 above, or of Okumura in view of Okada et al. and Yasunishi as applied to claim 8 above.

Second Set of Appliance Claims

As to claims 40, 42, 44, and 46, Yamazaki teaches a rear projector comprising three display devices Yamazaki, col. 16, lines 1 – 25; and figure 11. As to claims 47, 49, 51, and 53, Yamazaki teaches a front projector comprising three display devices. Yamazaki, col. 15, lines 32 – 56; and figure 10. As to claims 54, 56, 58, and 60, Holmes teaches a single plate type rear projector. Holmes, col. 8, lines 48 – 58. As to claims 61, 63, 65, and 67, Yamazaki teaches a goggle type display comprising two display devices. Yamazaki, col. 26, lines 38 – 40; and figure 22D. As to claims 68, 70, 72, 74, and 75, Kimura teaches a display for portable information terminal. Kimura, col. 1, lines 11 – 16. As to claims 76, 78, 80, and 82, Yun et al., teaches a notebook type personal computer. Yun, col. 1, lines 49 – 52; and figure 9. As to claims 90, 92, 94, and 96, Yamazaki teaches a mobile telephone. Yamazaki, col. 26, lines 26 – 29. As to claims 98, 100, 102, and 104, Yamazaki teaches a video camera. Yamazaki, col. 26, lines 29 – 33; and figure 22B. As to claims 106, 108, 110, and 112, Yamazaki teaches a mobile computer. Yamazaki, col. 26, lines 34 – 37; and figure 22C. As to claims 114, 116, 118, and 120, Munyan teaches a portable electric book. Munyan, col. 1, lines 56 – 57. As to claims 122, 124, 126, and 128, Kimura teaches a personal computer. Kimura, col. 1, lines 11 – 16. As to claims 130, 132, 134, and 136, Stambolic et al. teaches a electronic game device. Stambolic, col. 1, lines 9 – 10. As to claims 138, 140, 142, and 144, Kleinschmidt teaches an image reproduction device. Kleinschmidt, col. 5, lines 58 – 61. As to claims 146, 148, 150, and 152, Sato teaches a digital camera. Sato, col. 1, lines 7 – 10.

None of these patents specifically teach the display device of Okumura.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the display device of Okumura for these generally small appliances. Okumura teaches,

> The novel driving method of driving the active matrix circuits permits a high gray level display to readily be accomplished without a substantial enlargement of a circuit scale. Although the driver circuits and power supply circuits are simplified, the high gray level display is accomplished.

Okumura, col. 6, line 65 – col. 7, line 2.

16. Claims 9, 20, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over , in view of Okada et al as applied to claim 1 or claim 5 above, or of Okada et al and Yasunishi as applied to claim 3 or claim 7 above, and further in view of Wu et al., USPN 6,245,256 B1.

Claims 9, 20, 22, 24

Claims 9, 20, 22, and 24 add thresholdless antiferroelectric mixed liquid crystal indicating electro-optical characteristic of V-shape.

Okada does not teach thresholdless antiferroelectric mixed liquid crystal.

Wu teaches thresholdless antiferroelectric mixed liquid crystal indicating electro-optical characteristic of V-shape. Wu, col. 3, lines 2 –25; and figure 12.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the antiferroelectric mixed liquid crystal of Wu with the display device of Okada. Wu teaches,

> According to Inui's report, when the mixing ratio of I:II:III=40:40:20, no E_{th} value is found, and its field-induced antiferroelectric to ferroelectric switching shows a V-shaped switching (see FIG. 12). Inui give the name of "Thresholdless antiferroelectric liquid crystals; TLAFLCs" to this antiferroelectric liquid crystal mixture. These thresholdless antiferroelectric liquid crystals have the following properties:

(1) Great tilt angle (>35.degree.);

(2) Low driving voltage (<2V/μm^{-1});

(3) Ideal gray scale;

(4) Fast antiferroelectric to ferroelectric switching time (<50.mu.s);

(5) High contrast value (>100); and

(6) Broad viewing angle (>60.degree.).

The aforesaid properties eliminate the gray scale problem occurred during the fabrication of a passive matrix addressing (PM) surface stable ferroelectric liquid crystal display, and also improve the drawback of being difficult to obtain a high contrast ratio commonly existed in regular active matrix (AM) or thin film transistor (TFT) addressing type deformed-helix ferroelectric liquid crystal displays and passive matrix addressing type antiferroelectric liquid crystal displays.

Wu, col. 3, lines 2 –25.

17. Claims 19, 21, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura as applied to claim 2 above, or Okumura in view of Yasunishi as applied to claim 4 above, or Okumura in view of Okada et al as applied to 6 above, or of Okumura in view of Okada et al and Yasunishi as applied to claim 8 above, and further in view of Wu et al.

Claims 19, 21, 23, and 25

Claims 19, 21, 23, and 25 add thresholdless antiferroelectric mixed liquid crystal indicating electro-optical characteristic of V-shape.

Okumura does not teach thresholdless antiferroelectric mixed liquid crystal.

For the reasons stated in the discussion about claim 9 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the antiferroelectric mixed liquid crystal of Wu with the display device of Okumura.

18. Claims 18, 84, 85, and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable Okada et al as applied to claim 1 or claim 5 above, or of Okada et al and Yasunishi as applied to claim 3 or claim 7 above, and further in view of Bhargava, USPN 5,455,489.

Claims 18, 84, 85, and 87

Claims 18, 84, 85, and 87 teach an EL display.

Okada does not teach an EL display.

Bhargava teaches an EL display. Bhargava, col. 9, lines 46 – 64.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the EL display of Bhargava with the display device of Okada. Bhargava teaches,

> Today, EL displays offer unique properties such as flat-slim and high contrast but suffer from (1) poor efficiency, (2) limited color availability and control, (3) lack of gray scale, and (4) expensive drives for high voltage operation.
>
> As will be clear from the foregoing exposition, an EL display whose phosphor layer comprises a DNC particle layer will exhibit higher efficiency, improved gray scale, and due again to its tiny sized particles will operate at low voltages.

Bhargava, col. 9, line 60 – col. 10, line 2. This is especially true in light of Okada's invitation.

> Thus, the invention described herein makes possible the advantage of providing a driving circuit for a display apparatus, which has a simplified and small construction, and which can display an image with multiple gray scales in accordance with multi-bit video data.

Okada, col. 7, line 66 – col. 8, line 3.

19. Claims 83/2, 83/4, 86, and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura as applied to claim 2 above, or Okumura in view of Yasunishi as applied to claim 4 above, or Okumura in view of Okada et al as applied to 6 above, or of Okumura in view of Okada et al and Yasunishi as applied to claim 8 above, and further in view of Bhargava.

Claims 83/2, 83/4, 86, and 88

Claims 83/2, 83/4, 86, and 88 teach an EL display.

Okumura does not teach an EL display.

For the reasons stated in the discussion of claim 18, 84, 85, and 87 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the EL display of Bhargava with the display device of Okumura. This is especially true in light of Okumura's invitation.

> The novel driving method of driving the active matrix circuits permits a high gray level display to readily be accomplished without a substantial enlargement of a circuit scale. Although the driver circuits and power supply circuits are simplified, the high gray level display is accomplished.

Okumura, col. 6, line 65 – col. 7, line 2.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sakai et al., USPN 6,245,257 B1, teaches thresholdless antiferroelectric liquid crystal having a V shaped hysteresis curve.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

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DENNIS-DOON CHOW
PRIMARY EXAMINER